AMENDMENTS IN THE CLAIMS:

1.(previously presented): A finite impulse response (FIR) filter comprising:

a first operational unit for operating input data which including a first input data and a second input data inputted after the first input data, said input data consists of transmitting information and is composed of bit strings, and additional data which is added in order to transmit said input data and;

a second operational unit for operating on the first input data and a difference between said additional data corresponding to the first input data and said additional data corresponding to the second input data; and

an adding unit for adding results of the first and second operational units and outputting the resultant as a filter response.

2. (original) The FIR filter according to claim 1, further comprising

a data separation unit for separating data inputted to the filter into said input data and said additional data.

3.(previously presented): The FIR filter according to claim 1, further comprising:

a shift register for receiving said input data in sequence; and

factor multipliers for multiplying outputs from each of delay elements of said shift register by tap factors, and wherein:

said first operational unit includes a first adder tree for adding outputs from said factor multipliers and a first multiplier for multiplying an output from said first adder tree by said additional data;

said second operational unit includes a second adder tree for adding said first input data among said outputs from said factor multipliers and a second multiplier for multiplying an output from said second adder tree by said difference; and

said adding unit adds an output from said first multiplier and an output from said second multiplier.

4.(previously presented): The FIR filter according to claim 3, further comprising switches for connecting outputs of said factor multipliers to said second adder tree, wherein

said switches are switched on and off in response to a shift operation of said input data in said shift register and transmit said first input data to said second adder tree.

5. (original) The FIR filter according to claim 4, wherein

said switches are switched off in response to every shift operation of said shift register, the switching-off being performed in sequence, starting from a switch corresponding to one of said factor multipliers at an input side.

6.(previously presented): The FIR filter according to claim 3, further comprising switches for connecting said second adder tree to one of an output of a predetermined one of said factor multipliers and an output of a predetermined one of adders which compose said first adder tree, wherein

said switches are switched on and off in response to a shift operation of said input data in said shift register and transmit said first input data to said second adder tree.

7.(previously presented): The FIR filter according to claim 1, further comprising:

a holding circuit for accepting said additional data in response to a change in said input data and holding the accepted data as said additional data corresponding to said first input data; and

an operational circuit for operating a difference between said additional data outputted from said holding circuit and new additional data.

8.(previously presented): A finite impulse response (FIR) filter comprising:

a first operational unit for operating on a second input data inputted after a first input data among input data which includes the first input data and the second input data and consists of transmitting information and is composed of bit strings, and additional data which is added in order to transmit the second input data;

a second operational unit for operating on the first input data and said additional data corresponding to said first input data; and

an adding unit for adding results of the first and second operational units and outputting the resultant as a filter response.

9. (original) The FIR filter according to claim 8, further comprising

a data separation unit for separating data inputted to the filter into said input data and said additional data.

10. (original) The FIR filter according to claim 8, further comprising:

a shift register for receiving said input data in sequence;

factor multipliers for multiplying outputs from each of delay elements of said shift register by tap factors; and

switches being switched on and off in response to a shift operation of said input data in said shift register, for transmitting outputs from said factor multipliers to one of said first operational unit and said second operational unit.

11-14.(cancelled)

15.(previously presented): A method of operating a finite impulse response (FIR) filter, comprising the steps of:

receiving in sequence input data which includes a first input data and a second input data inputted after the first input data, said input data consists of transmitting information and is composed of bit strings;

operating said input data and additional data which is added in order to transmit said input data;

operating the first input data and a difference between said additional data corresponding to said first input data and said additional data corresponding to the second input data; and

adding results of said operations and outputting the resultant as a filter response.

16.(previously presented): A method of operating a finite impulse response (FIR) filter, comprising the steps of:

receiving in sequence input data which includes a first input data and a second input data inputted after the first input data, said input data consists of transmitting information and is composed of bit strings;

operating the second input data and additional data which is added in order to transmit said second input data;

operating the first input data and said additional data corresponding to said first input data; and

adding results of said operations and outputting the resultant as a filter response.

17.(cancelled):

18.(previously presented): A semiconductor integrated circuit including a finite impulse response (FIR) filter, wherein

the FIR filter comprises:

a first operational unit for operating input data which includes a first input data and a second input data inputted after the first input data, said input data consists of transmitting information and is composed of bit strings, and additional data which is added in order to transmit said input data;

a second operational unit for operating the first input data and a difference between said additional data corresponding to the first input data and said additional data corresponding to the second input data; and

an adding unit for adding results of the first and second operations and outputting the resultant as a filter response.

19.(previously presented): A semiconductor integrated circuit including a finite impulse response (FIR) filter, wherein

the FIR filter comprises:

a first operational unit for operating a second input data inputted after a first input data among input data which includes the first input data and the second input data, said input data consists of transmitting information and is composed of bit strings, and additional data which is added in order to transmit said second input data;

a second operational unit for operating the first input data and said additional data corresponding to said first input data; and

an adding unit for adding results of the first and second operations and outputting the resultant as a filter response.

20.(cancelled)

21.(currently amended): A ~~finite impulse response (FIR) filter~~ transmission circuit for use in a communication system comprising:

a first operational unit for operating input data which includes a first input data and a second input data inputted after the first input data, said input data consists of transmitting information and is composed of bit strings, and additional data which is added in order to transmit said input data;

a second operational unit for operating the first input data and a difference between said additional data corresponding to the first input data and said additional data corresponding to the second input data; and

an adding unit for adding results of the first and second operations and outputting the resultant as a filter response.

22.(currently amended): A ~~finite impulse response (FIR) filter~~ transmission circuit for use in a communication system comprising:

a first operational unit for operating a second data inputted after a first input data among input data which includes the first input data and the second input data, said input data consists of transmitting information and is composed of bit strings, and additional data which is added in order to transmit said second input data;

a second operational unit for operating the first input data among said input data and said additional data corresponding to said first input data; and

an adding unit for adding results of said first and second operations and outputting the resultant as a filter response.

23.(cancelled)